AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph immediately after the title on page 1 as follows:

This application is a divisional of application no. 10/078,418, filed February 21, 2002, now U.S. Patent No. 6,717,459, issued April 6, 2004, the entire disclosure of which is incorporated herein by reference.

Please amend the paragraph beginning at page 9, line 24 as follows:

Four charge pump phase circuits are shown in Figs. 4A and 4B: a first phase circuit 202, a second phase circuit 204, a third phase circuit 206, and a fourth phase circuit 208. In the first phase charge pump circuit 202, a first bootstrap capacitor 210 includes first 212 (driving side) and second 214 (driven side) terminals. In the same fashion described above with respect to the two phase charge pump, the bootstrap capacitor 210 is driven on its driving side 212 by a driver circuit 218. During discharge, capacitor 210 transfers charge through an equalization circuit B 300 to a bootstrap capacitor 250 of phase circuit 206. The illustrated embodiment includes an ancillary pump circuit 229 associated with the first phase charge pump circuit 202. This ancillary pump circuit 229 includes a first ancillary capacitor 231 having third 232 (driving side) and fourth 234 (driven side) terminals. The third terminal 232 is operatively connected to an output 236 of a second driver circuit 238. As would be understood by one of skill in the art, the ancillary pump circuit 229 serves to elevate the output voltage supplied to a load 38 by applying an elevated voltage to a gate 230 of an output transistor 228. During operation, the voltage on the driven side 214 of bootstrap capacitor 210 rises above VCC 12. In response, current flows through diode connected transistor 239, and charges the driven side 234 of ancillary capacitor 231 to a voltage above VCC.

Thereafter, the driving side 232 of ancillary capacitor 231 is raised from ground potential to VCC 12. The result is that the voltage applied to the gate 230 of the output transistor 228 is high enough to allow the full voltage on the driven side 214 of bootstrap capacitor 210 to reach the input of the load 38. The first ancillary capacitor 231 also serves to supply additional charge to the load 38 by transferring charge through transistor ~~240~~ 290 to the driven side 214 of capacitor 210 when the voltage thereon falls below a design threshold.

Please amend the paragraph starting on page 10, line 22 as follows:

The circuitry of the first phase circuit 202 is duplicated in the second 204, third 206, and fourth 208 phase circuits and the operation of these additional phase circuits is the same as that of circuits 202 and 229 as would be clear to one of skill in the art in light of the description provided above. The outputs of each of the four phase circuits 202, 204, 206, 208 are mutually connected at an output node VP2. ~~242.~~ In each phase circuit, a primary charge pump with a primary bootstrap capacitor is supplemented by an ancillary charge pump with an ancillary bootstrap capacitor. The respective ancillary charge pump serves to provide an elevated voltage to a gate of an output transistor of the primary charge pump, and to supply charge to the output of the primary charge pump via a pair of bridge transistors once the voltage on the driven side of the respective primary bootstrap capacitor begins to fall. According to one aspect of the invention, as shown, charge is shared between bootstrap capacitors 231 and 286 through an equalization circuit D 301, between capacitors 231 and 280 through an equalization circuit C 303, between capacitors 280 and 260 through an equalization circuit E 305, between capacitors 260 and 286 through an equalization circuit F 307, and between capacitors 287 and 291 through an equalization circuit A 309.

Please amend the paragraph beginning on page 12, line 6 as follows:

Similarly, signals C0, C1, C1_, C2, C2_, C3, and C3_ ~~the four signals C0_, C1_, C2_, and C3_ produced by circuit portion 400~~ are applied to combinational logic 440 to produce 12 control signals B0P, B0P_, B0N, B1P, B1P_, B1N, B2P, B2P_, B2N, B3P, B3P_, and B3N that control the four inverters driving the four respective ancillary bootstrap capacitors 231, 280, 260, and 286 as shown in figures 4A and 4B.

Please amend the paragraph beginning on page 12, line 11 as follows:

Together, the timing circuit 400 and the two combinational logic circuit portions 430 and 440 serve to operate the four phase circuits, including ancillary circuits, of the charge pump of figures 4A and 4B such that the potentials on the bootstrap capacitors, as seen at the mutual VP2 ~~output 242~~ of the four phase circuits, are at respective phase angles of 0, 90, 180, and 270 degrees.